l'Observatoire de Paris — LESIA
Laboratoire d'Études Spatiales et d'Instrumentation en Astrophysique

Durham University

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Green Flash

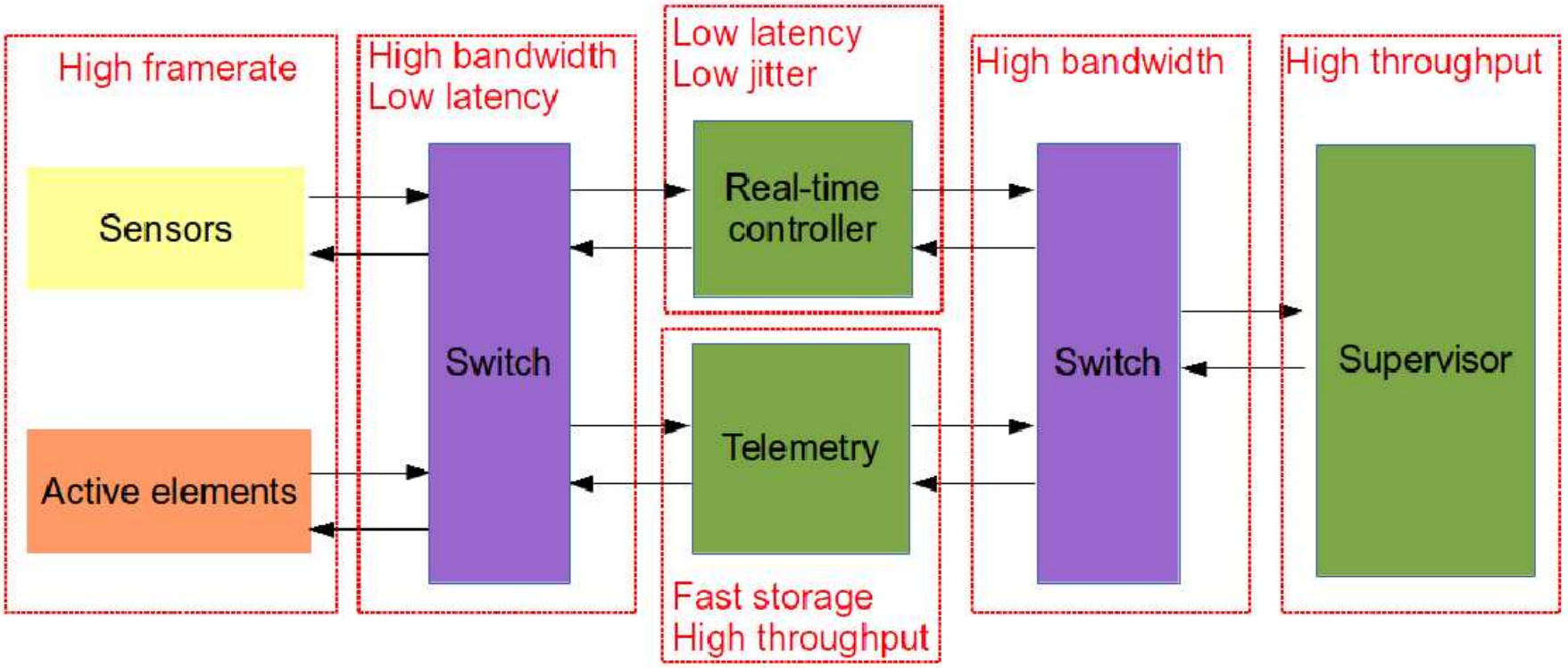
High performance computing for real-time science

Project overview and management (WP 1 & 2)

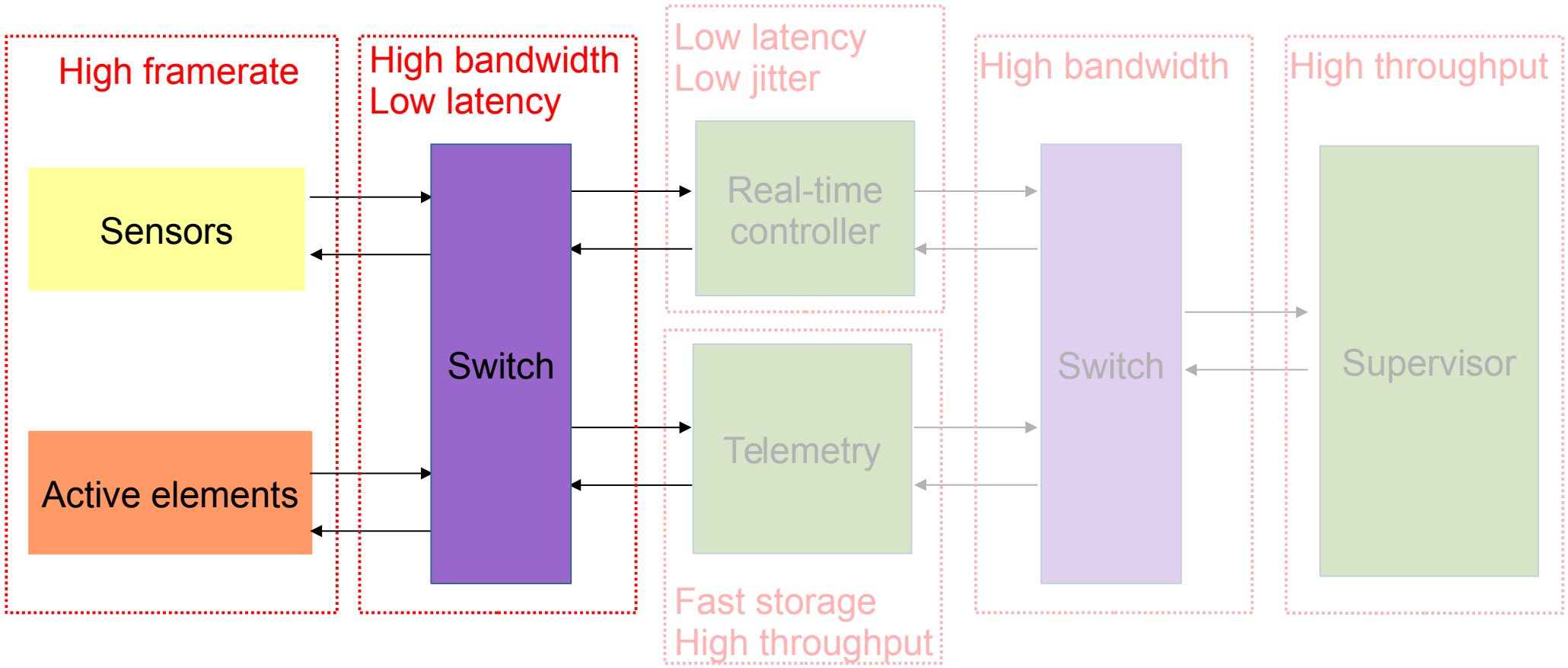
European Commission

Project #671662 funded by European Commission under program H2020-EU.1.2.2 coordinated in H2020-FETHPC-2014

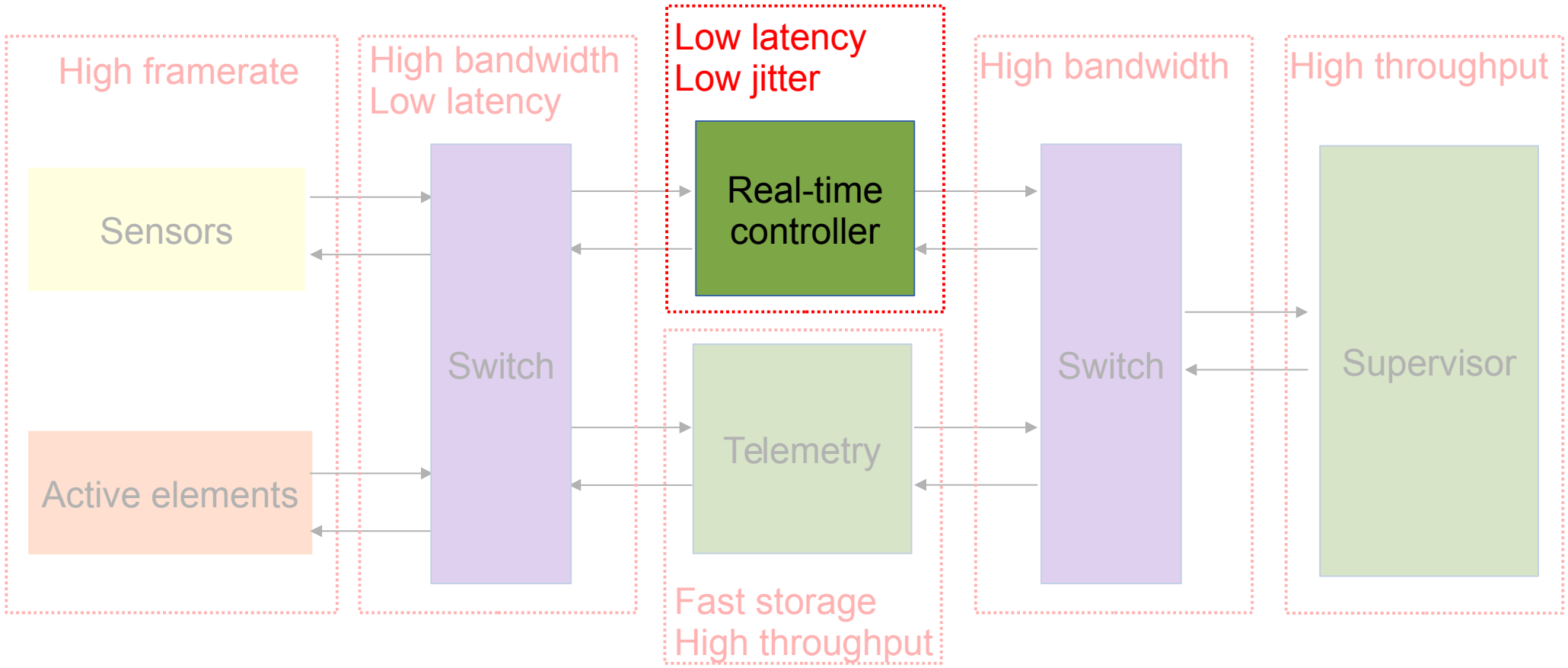
AO RTC concept



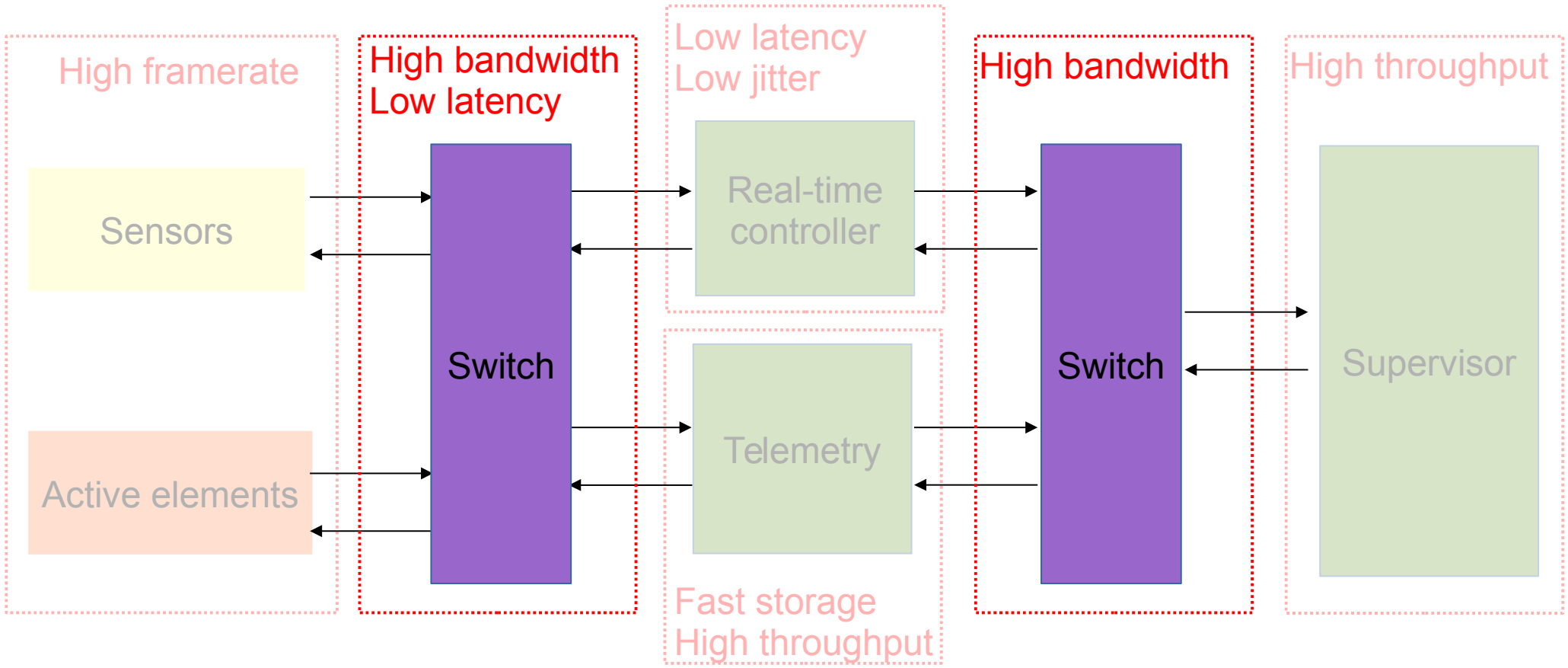
AO RTC concept : RT simulator



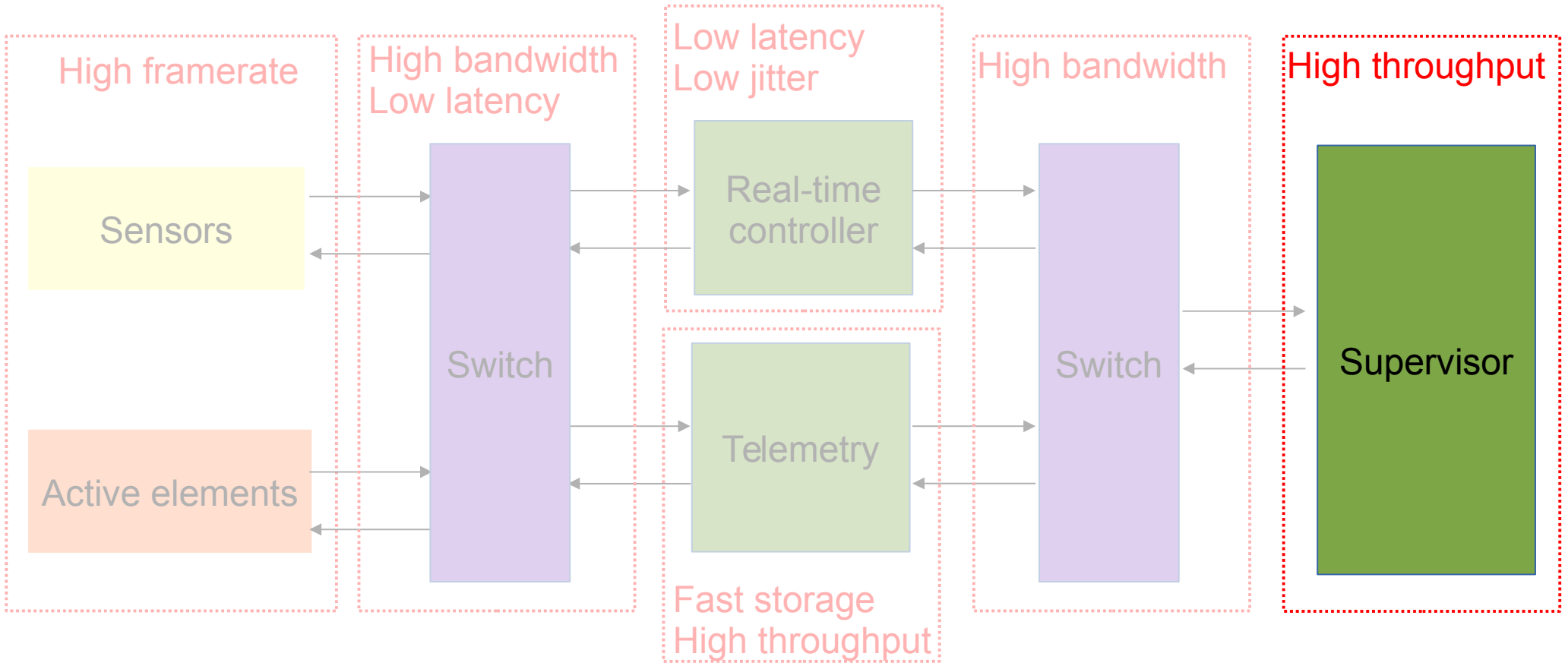
AO RTC concept : data pipeline



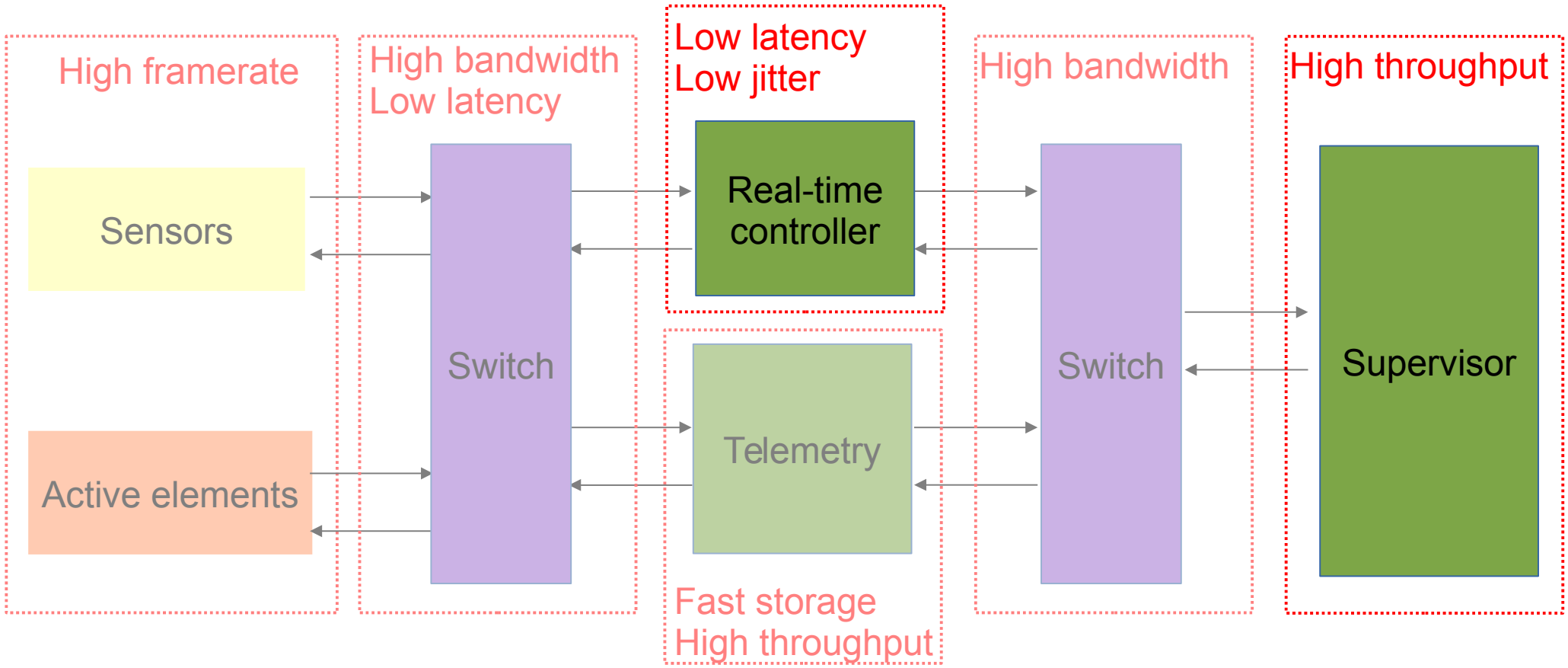
AO RTC concept : smart interconnect



AO RTC concept : supervisor



AO RTC concept : SW & MW



Introduction to Green Flash

- Program objectives: 3 research axes
  - 2 technological developments and 1 validation study
- Real-time HPC using accelerators and smart interconnects
  - Assess the determinism of accelerators performance
  - Develop a smart interconnect strategy to cope for strong data transfer bandwidth constraints
- Energy efficient platform based on FPGA for HPC
  - Prototype a main board, based on FPGA SoC and PCIe Gen3
  - Cluster such boards and assess performance in terms of energy efficiency and determinism
- AO RTC prototyping and performance assessment
  - Assemble a full functionality prototype for a scalable AO RTC targeting the MAORY system
  - Compare off-the-shelf solutions based on accelerators and new FPGA-based concept

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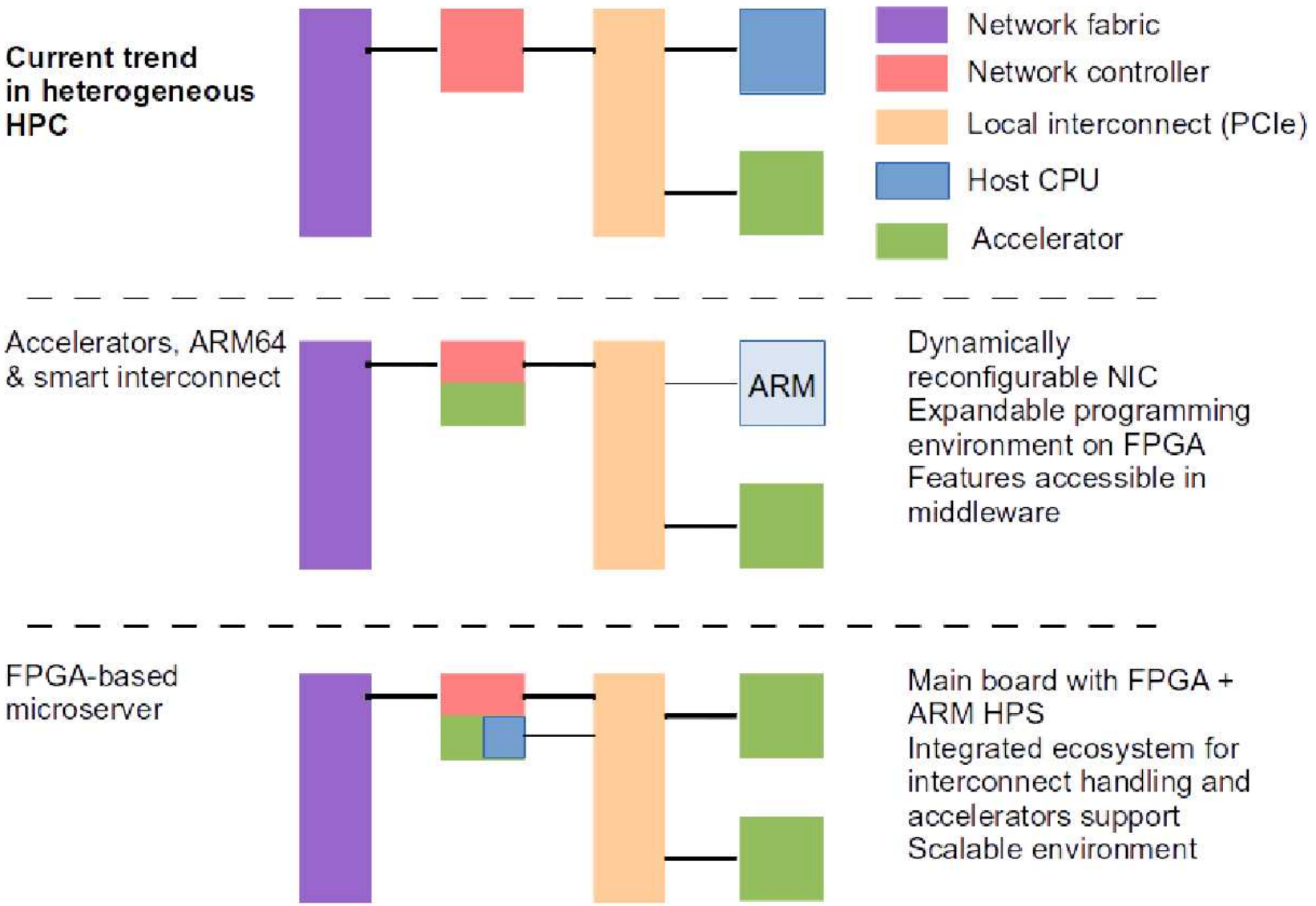
What this is about … really

- Find the best trade-off for ELT sized AO systems RTC
  - Comprehensive assessment of existing technologies
  - Development of new custom solutions for comparison
  - Propose new development processes to reduce cost and increase maintainability
- Build a full featured RTC prototype at the largest scale possible
  - Technology down-selection from a number of criteria : performance, cost, compliance to standards, obsolescence, maintainability
  - State of the art system to be assessed in the llab, with a simulator

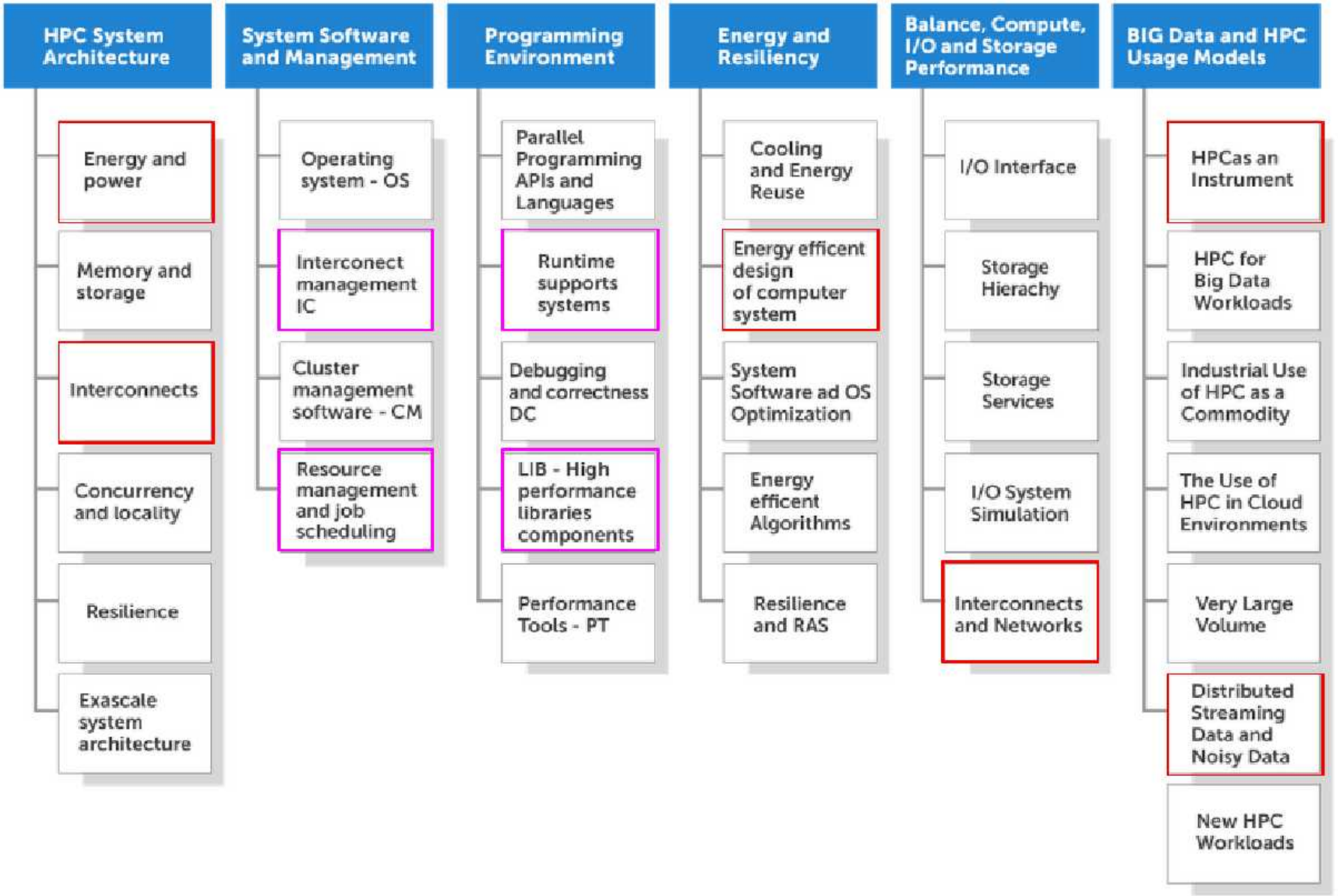
Objectives of Green Flash

- Real-time HPC using accelerators and smart interconnects
  - (1.1) Prototype cluster : 1.5 TMAC/s, 250 Gb/s of streaming data, max. jitter of 100µs of 1 sec of operations based on COTS accelerators
  - (1.2) Develop COTS NIC solution based on FPGA (TCP/UDP through 10G Ethernet)
  - (1.3) Complement FPGA development tool (QuickPlay) ecosystem with data handling and computing blocks for smart interconnect strategy
  - (1.4) Assess performance of linear algebra (MVM, Cholesky facto.) on prototype cluster
- Energy efficient platform based on FPGA for HPC
  - (2.1) Prototype a main board, based on FPGA SoC (Arria 10), including PCIe Gen3 and 10G Ethernet
  - (2.2) Provide support for this board in QuickPlay, including smart interconnect features
  - (2.3) Cluster such boards and assess performance in terms of energy efficiency and determinism on linear algebra + streaming data
- AO RTC prototyping and performance assessment
  - (3.1) Assemble a full functionality prototype for a scalable AO RTC targeting the MCAO system on E-ELT
  - (3.2) Implement a real-time simulator for performance assessment
  - (3.3) Fully characterize the AO RTC prototype performance under realistic conditions with simulator

Assessing new HPC concepts



Addressing HPC roadmap to exascale



Green Flash project

- Partners
  - 2 academic partners
    - LESIA, Observatoire de Paris, P.I. Damien G.
    - CfAI, University of Durham
  - 2 industrial partners
    - Microgate : Italian SME designing FPGA solutions for various applications (including astronomical AO)
    - PLDA: French SME developing FPGA solutions (mostly IP cores, world leader in PCIe IP)

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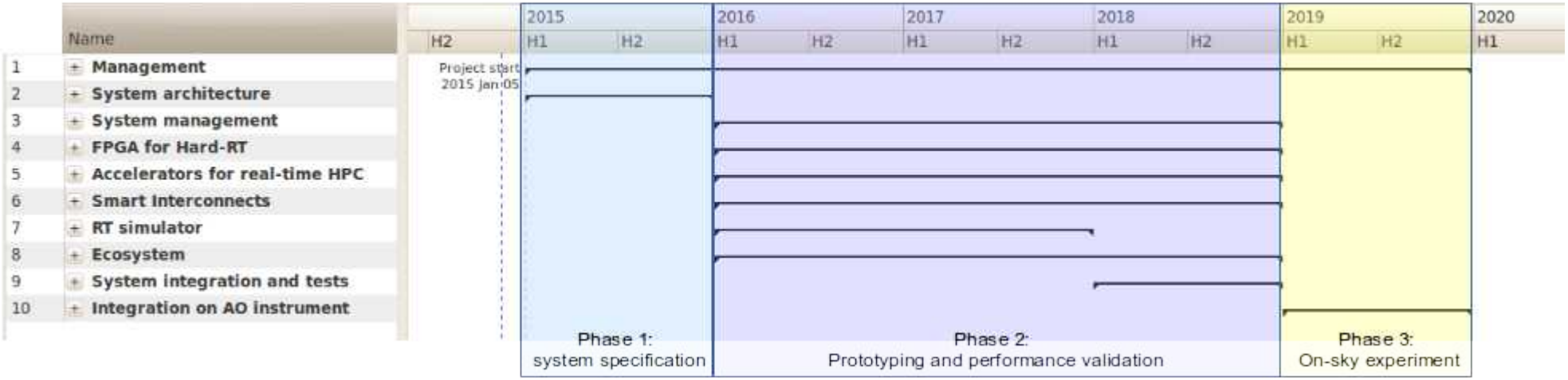
Project Management

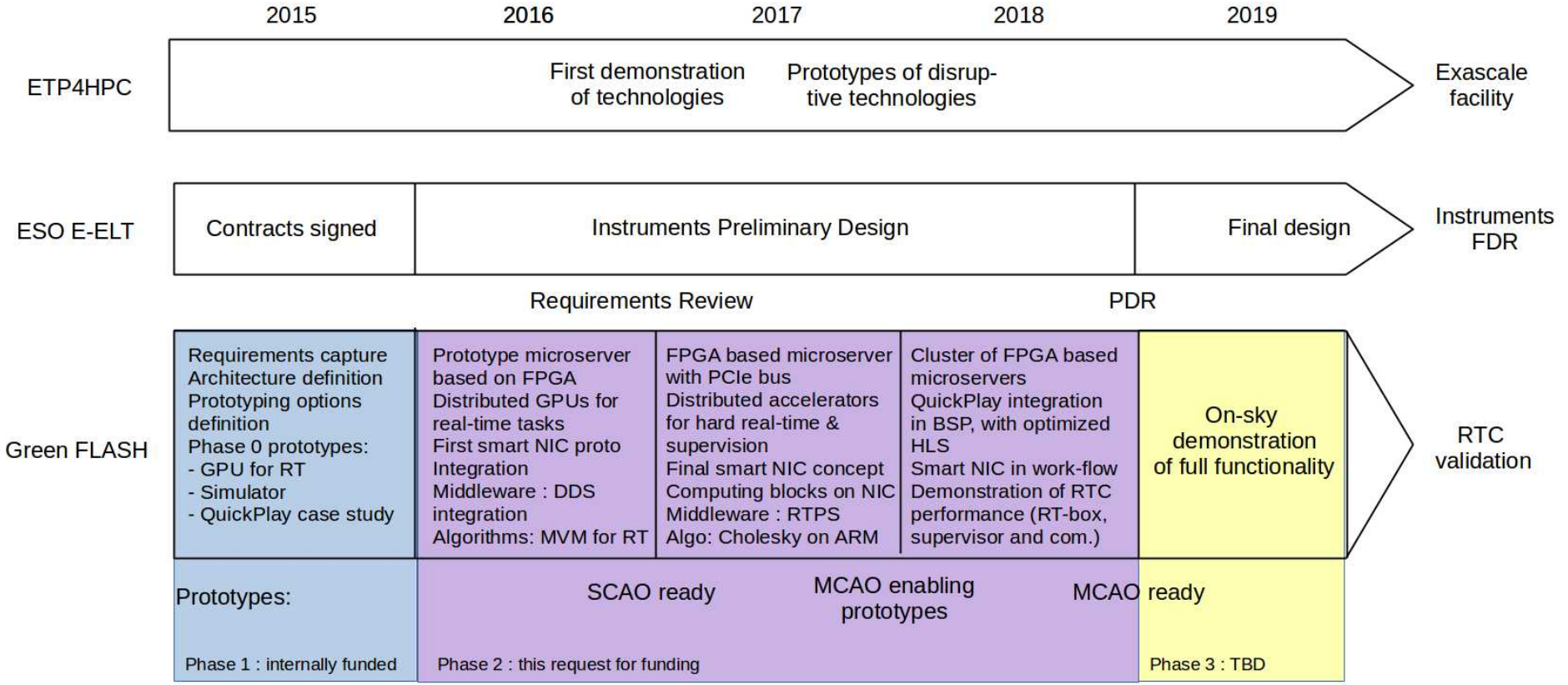
3 phases. Phase 2 funded through H2020 program

- Main prototyping phase from system specifications
- On-sky experiment to be defined along the course of the project



Project Management

- Good convergence with H2020 ETP4HPC / E-ELT project timeline



Work Packages

WP1: Project management (OdP)

WP2: System management (OdP)

WP3: FPGA for hard-RT (Mic)

WP4: Accelerators for real-time HPC (OdP)

WP5: Smart interconnect (PLDA)

WP6: RT simulator (UoD)

WP7: Ecosystem (UoD)

WP8: System integration and tests (UoD)

WP9: Integration on AO instrument (UoD)

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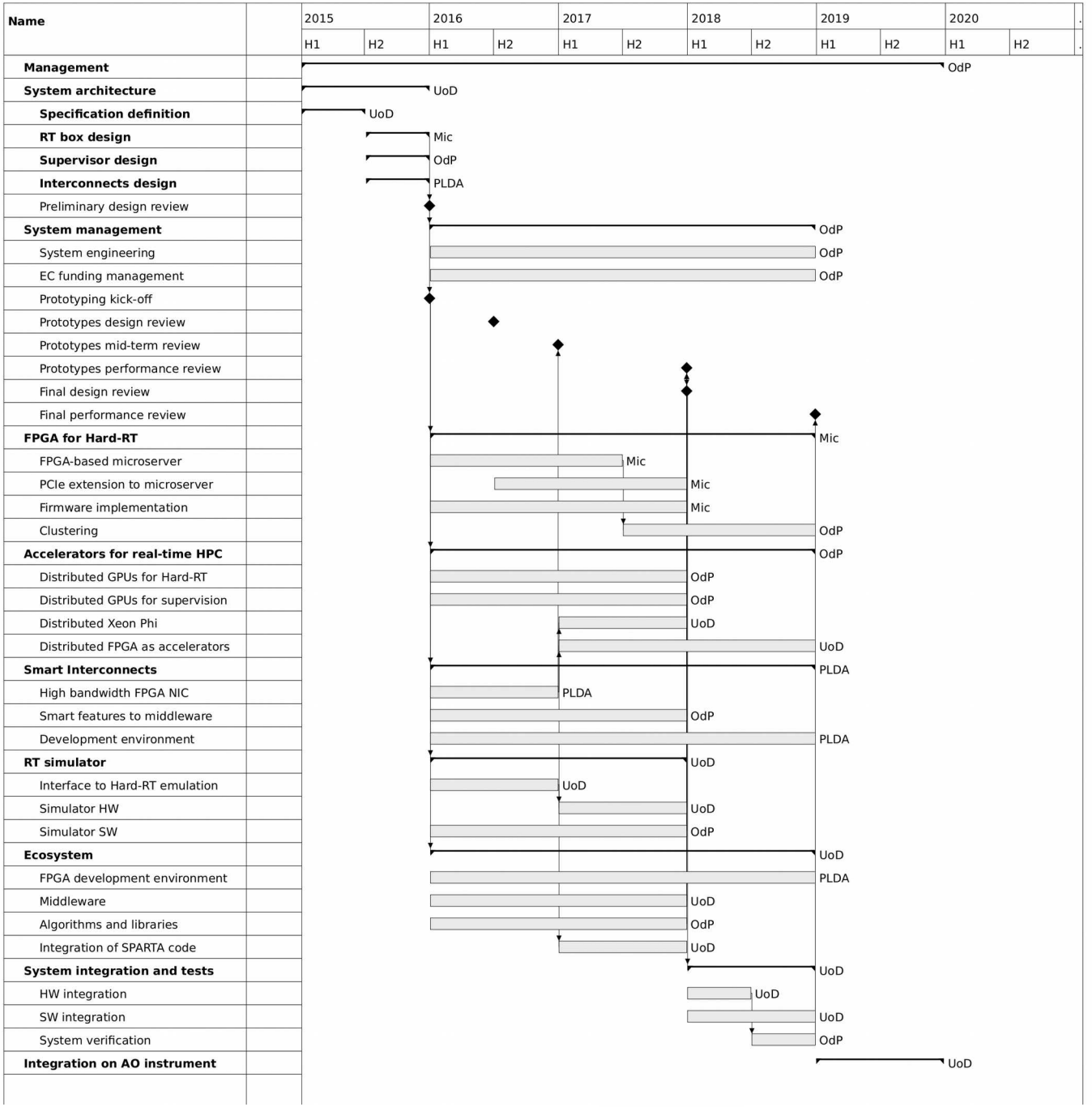
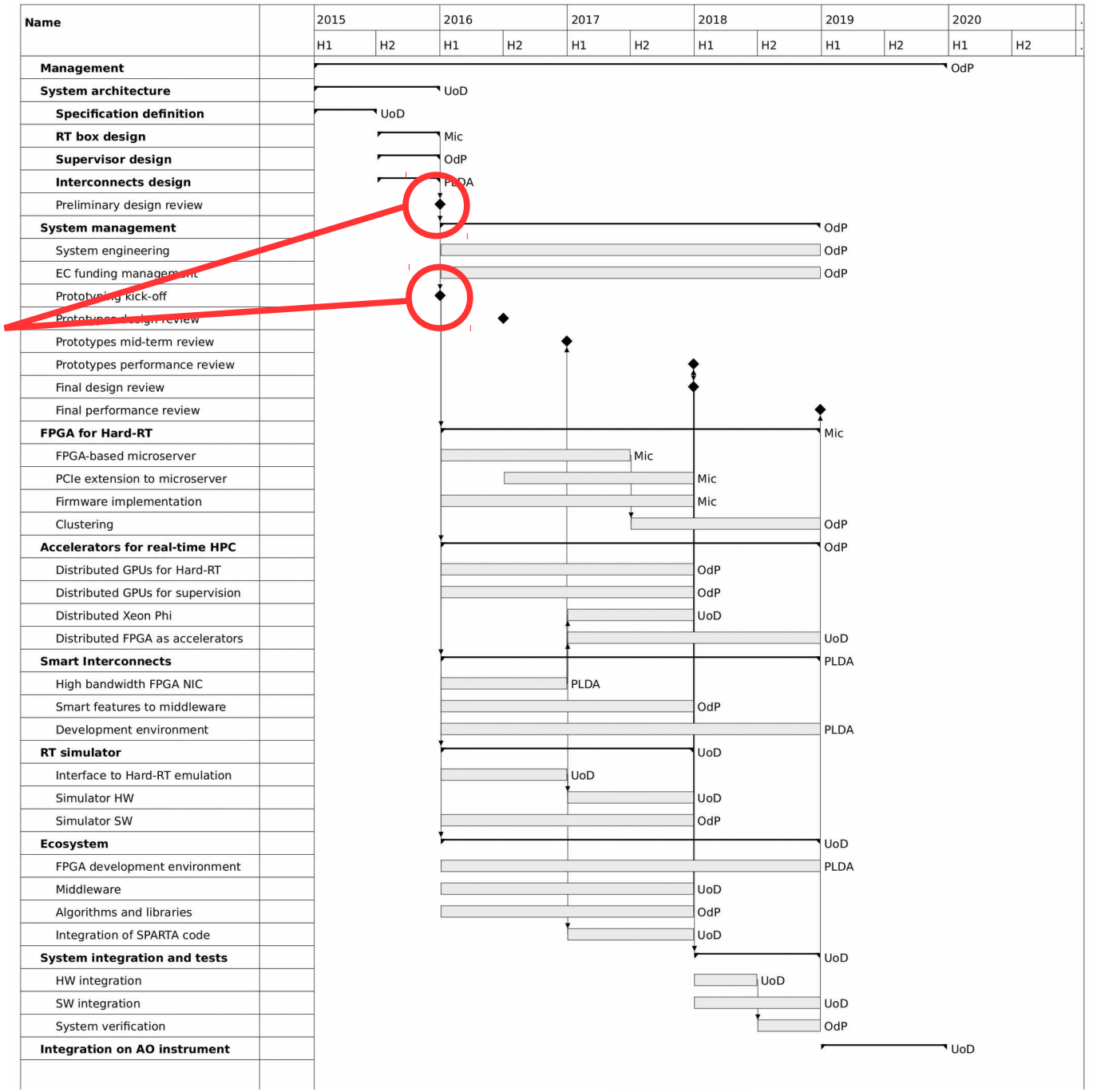
WP1


Name
2015
2016
2017
2018
2019
2020
H1
H2
Management
System architecture
Specification definition
RT box design
Supervisor design
Interconnects design
Preliminary design review
System management
System engineering
EC funding management
Prototyping kick-off
Prototypes design review
Prototypes mid-term review
Prototypes performance review
Final design review
Final performance review
FPGA for Hard-RT
FPGA-based microserver
PCIe extension to microserver
Firmware implementation
Clustering
Accelerators for real-time HPC
Distributed GPUs for Hard-RT
Distributed GPUs for supervision
Distributed Xeon Phi
Distributed FPGA as accelerators
Smart Interconnects
High bandwidth FPGA NIC
Smart features to middleware
Development environment
RT simulator
Interface to Hard-RT emulation
Simulator HW
Simulator SW
Ecosystem
FPGA development environment
Middleware
Algorithms and libraries
Integration of SPARTA code
System integration and tests
HW integration
SW integration
System verification
Integration on AO instrument
OdP
UoD
Mic
PLDA

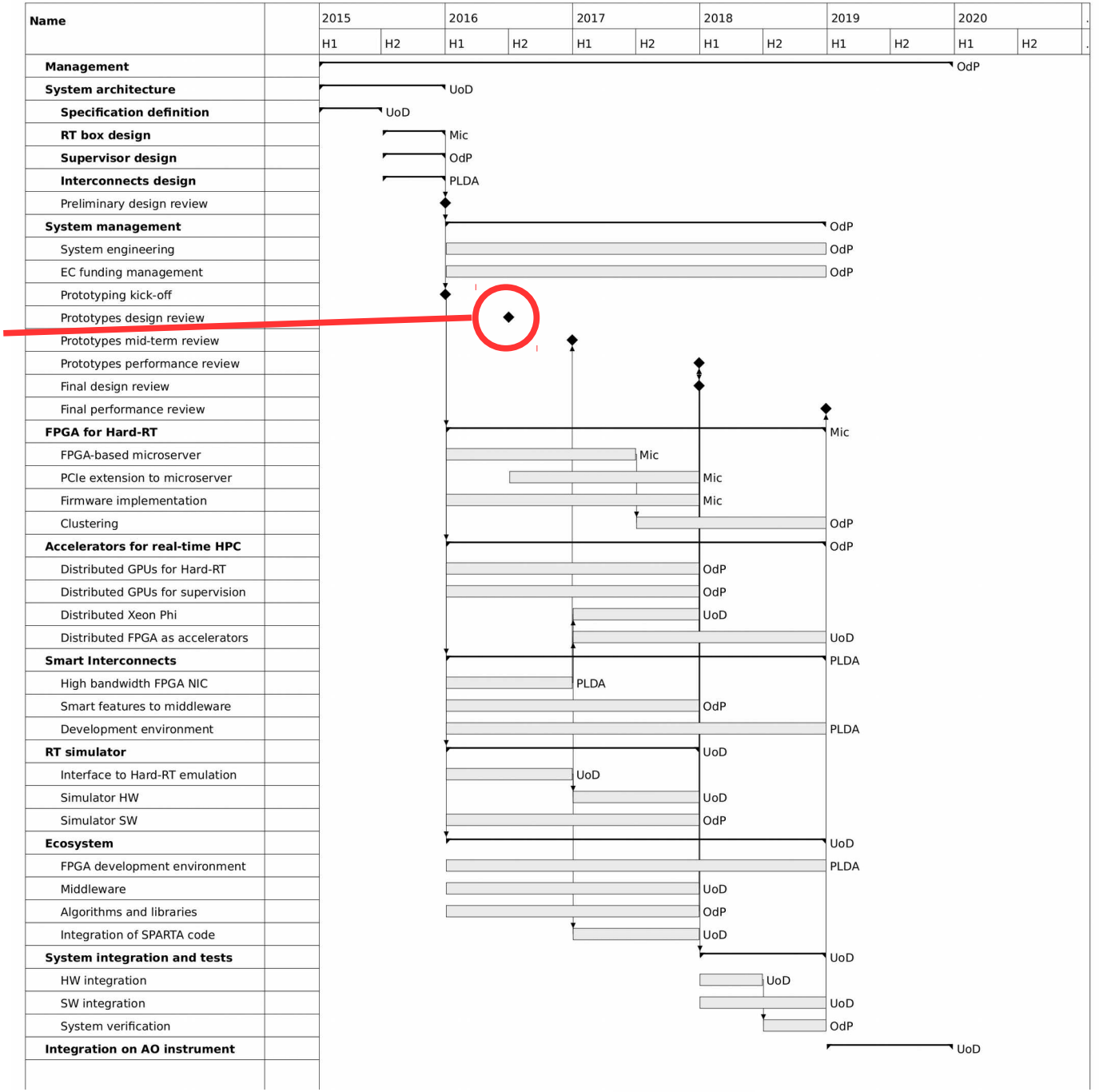
WP1

- Preliminary design review
- Held on 22nd Jan. 2016
- Review panel from E-ELT instruments community and AO RTC specialist
- Design documentation for all prototyping activities
- Including E-ELT AO RTC specification capture



WP1

- Prototypes design review
- Slightly delayed due to unavailability of components (FPGA)
- Could not happen between Oct. and Nov. 2016
- Prototyping activities have started on the basis of PDR results
- 9 months check review in Brussels did the job

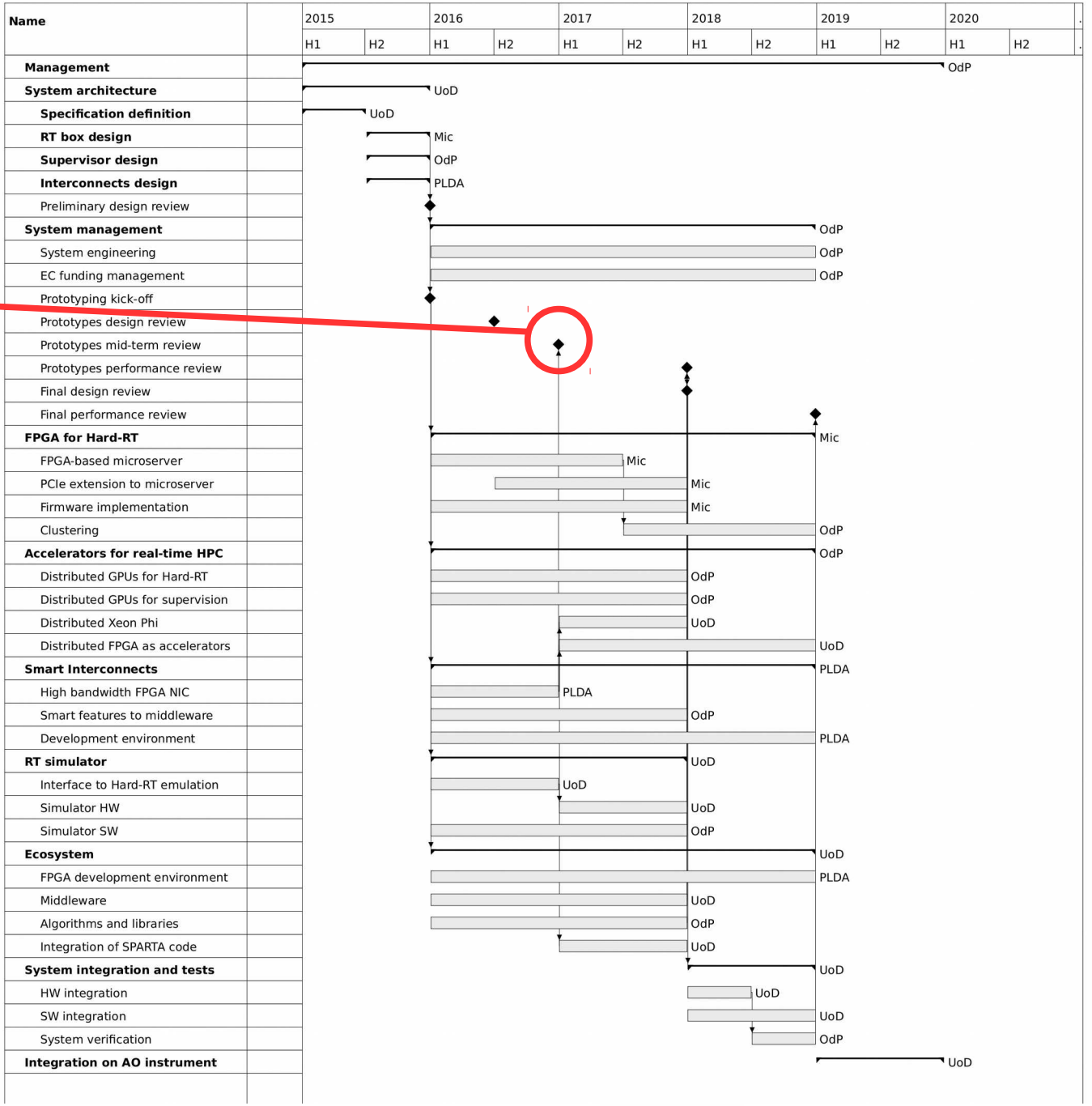


WP1

Prototyping mid-term review

Today !

2-3 months delay

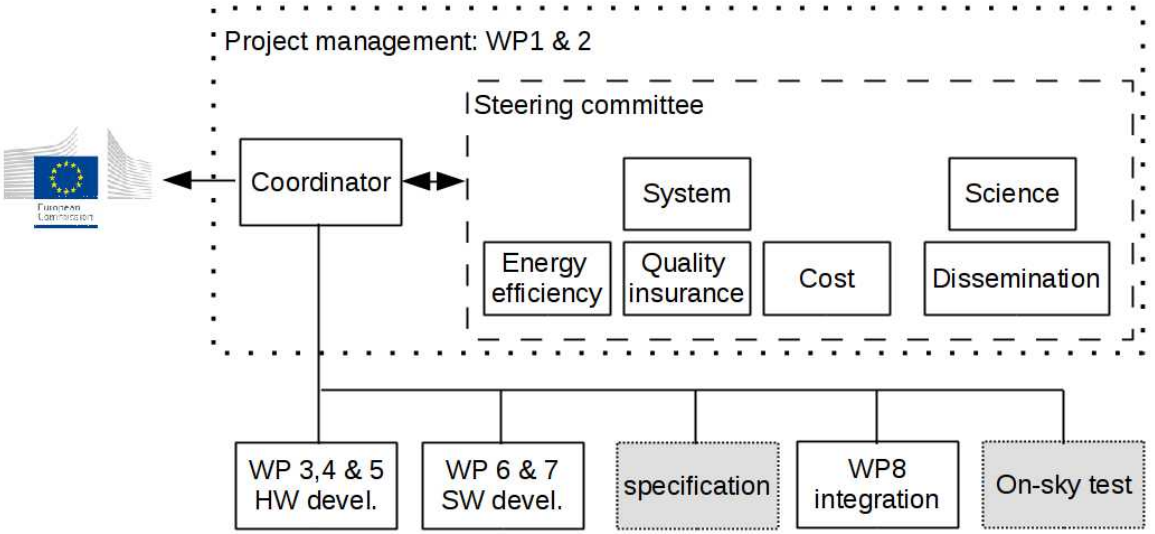


01/22/2016

WP1: project management

Task 1.1: project management (OdP)

- Coordination of steering committee
- Meeting on a monthly basis



Deliverables

- D1.6: data management plan (OdP – M6) : **descoped**
- D1.7: project periodic report 1 (OdP – M18 moved to M24)
- D1.8: project periodic report 2 (OdP – M36)
- D1.9: project final report (OdP – M36)

WP1: project management

Task 1.2: Dissemination strategy

Science activities

Publication / communication strategies

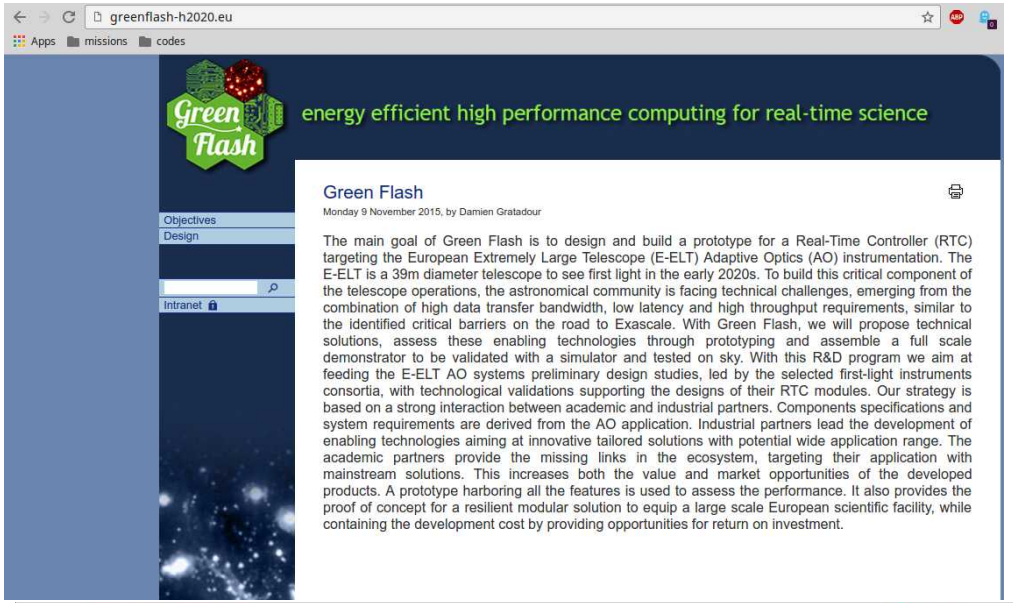
Strategy for on-sky experiment

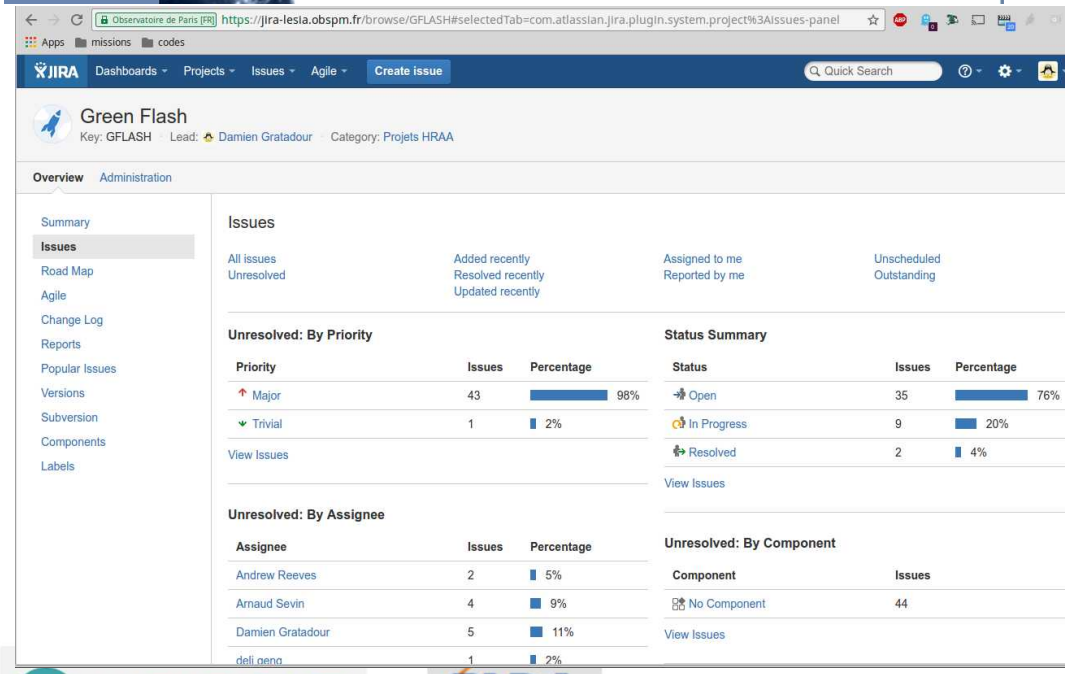
Deliverables:

- D1.1: project internal website (OdP – M6)
- D1.2: project public website (OdP – M6)

Contribution from OdP : >50%

WP will run over the course of the project





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WP1: project management

Communication:

- Project presented at EXDCI workshop during European HPC summit week (May 2016)
- Project presented at GPU technology conference (April 2016)
  - Blog post on NVIDIA website : https://blogs.nvidia.com/blog/2016/05/23/reshaping-light-rays-with-gpus/

Publications

- 3 contributions to SPIE conference on astronomical telescopes and instrumentation (Edinburgh, June 2016, to be published)
  - Gratadour et al. : overview of the project
  - Perret et al. : interconnect prototyping
  - Ferreira et al. : simulations and error budget
- Several submissions to AO4ELT5 and several papers in prep.

Meeting organized with E-ELT instrument consortia representatives at the SPIE conference

- MICADO, HARMONI, MAORY, METIS
- Status update and feedback on PDR panel comments

WP1: project management

Task 1.3: Energy efficiency (Mic)

Definition of criteria to assess energy efficiency

Lead the monitoring of energy efficiency for each sub-system and report

Deliverables :

- D1.3: Energy efficiency report (Mic – M36)

Task 1.4: Quality insurance (PLDA)

Management of the development process to secure quality of deliverables

Description of environments and promoted standards

Deliverables

- D1.4: Development process report (PLDA – M36)

Task 1.5: Cost reduction (Mic)

Lead a market survey to identify trends

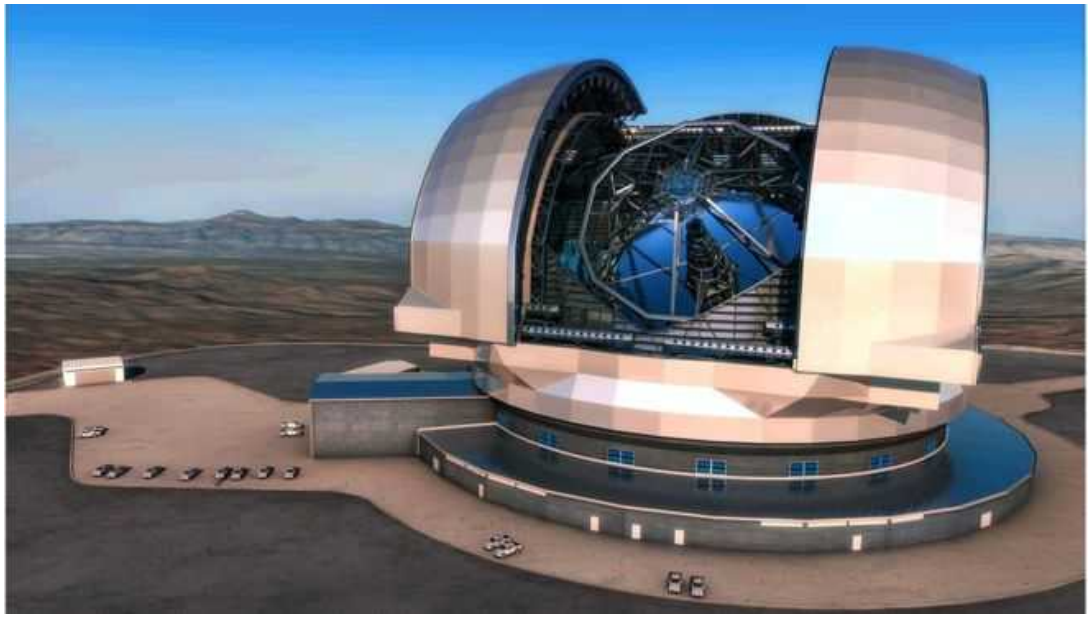
Procedures to monitor production cost and reporting

Deliverables

- D1.5: Cost projection report (Mic – M36)

Interaction with external partners

- Follow up on E-ELT instruments design specifications
  - After PDR, mid-term review
  - Welcome interactions as much as possible
  - Output of PDR presented at SPIE conference in June 2016



- Collaboration with ESO
  - Welcome interaction as much as possible (ESO representative participating to steering committee meetings as observer)
  - Part of standards will become public by mid 2017

Interaction with external partners

Collaboration with FET-HPC projects

- Green Flash is peculiar: real-time HPC, close to instrumentation
- FPGA technology as an option : similarities with MANGO project
- First meeting in June 2016
  - Brainstorming around projects goals and possible collaboration
  - First iteration by Sept. 2016 to define some technical

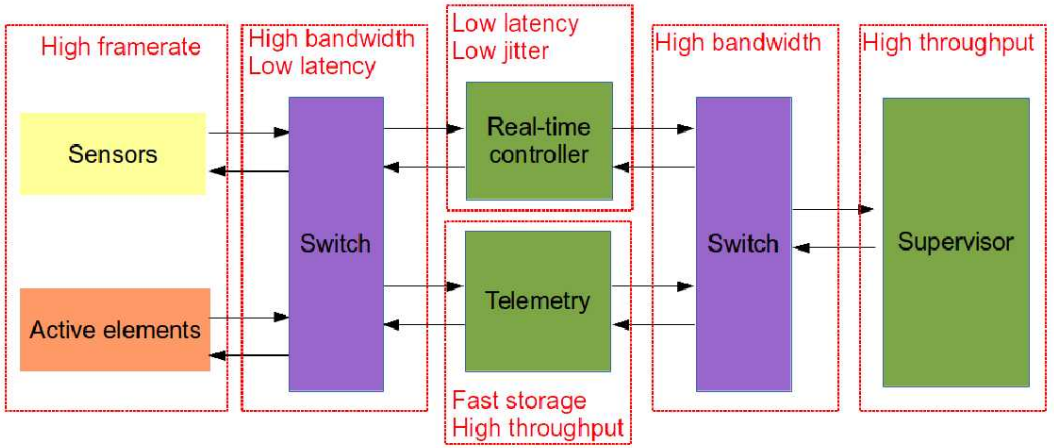
Collaboration with other partners

- Collaboration with Extreme Computing Research Center (ECRC) @KAUST on optimized linear algebra
  - Several papers published and in preparation
  - Co-supervision of PhD thesis
- Collaboration with U.K. Astronomy Technology Center on other applications / technologies for real-time HPC to be initiated
- Welcome collaborations (discussion with BSC around simulator upgrade, more collaborations in astronomy are being discussed, etc ..)

WP2: system management

Task 2.1: System architecture

- Requirements capture and specification definition
- Strategies for RT box, supervisor and interconnect



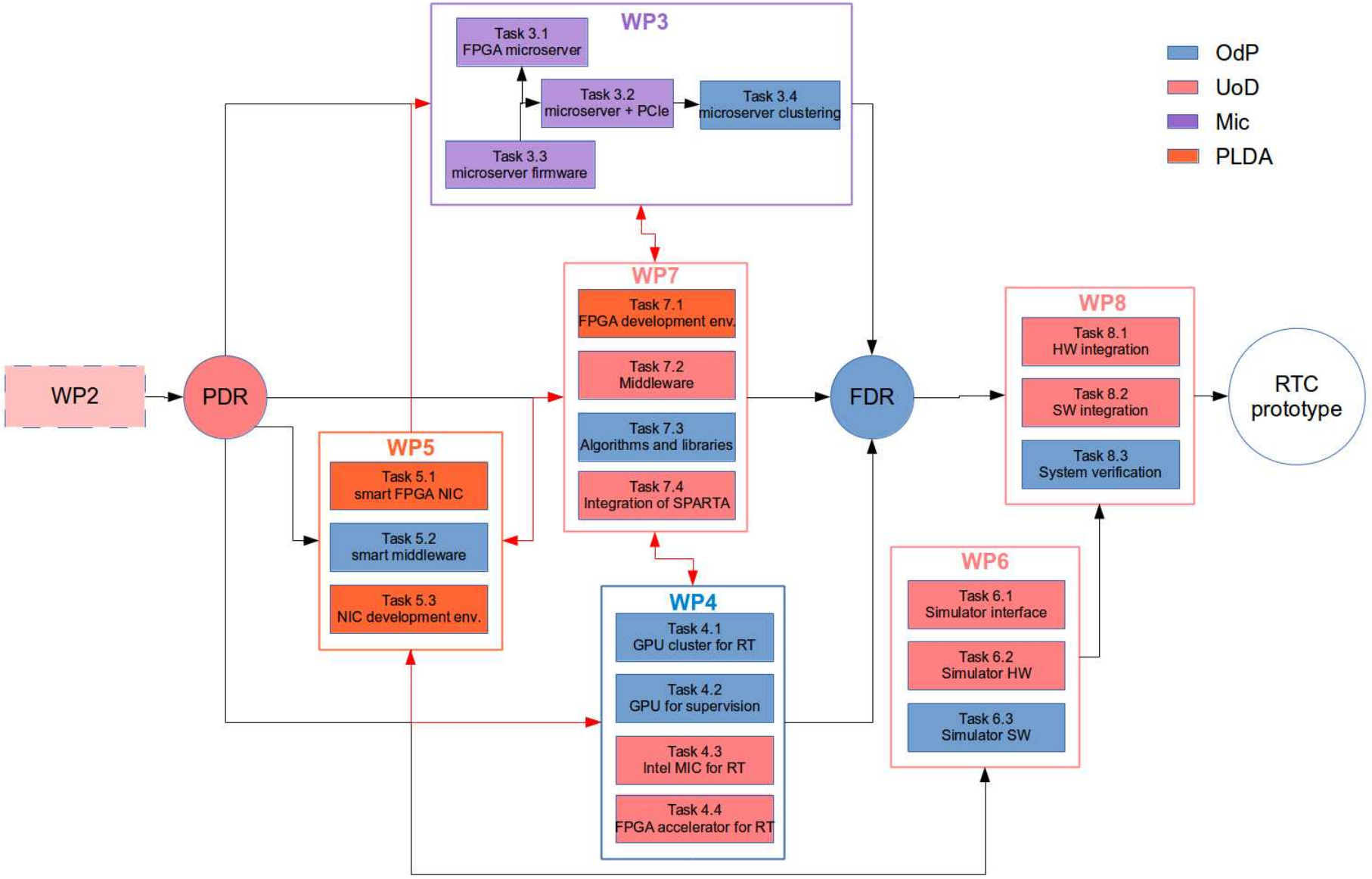
Deliverables (all internal):

- D2.1a: requirements document (UoD - M6)
- D2.1b: preliminary design document (UoD – M12)
- D2.1c: RTC box architectural options definition (Mic – M12)
- D2.1d: Supervisor module architectural options definition (OdP – M12)
- D2.1e: Interconnect strategies definition document (PLDA - M12)

Preliminary Design review held on January 2016

- PDR documentation + feedback from panel

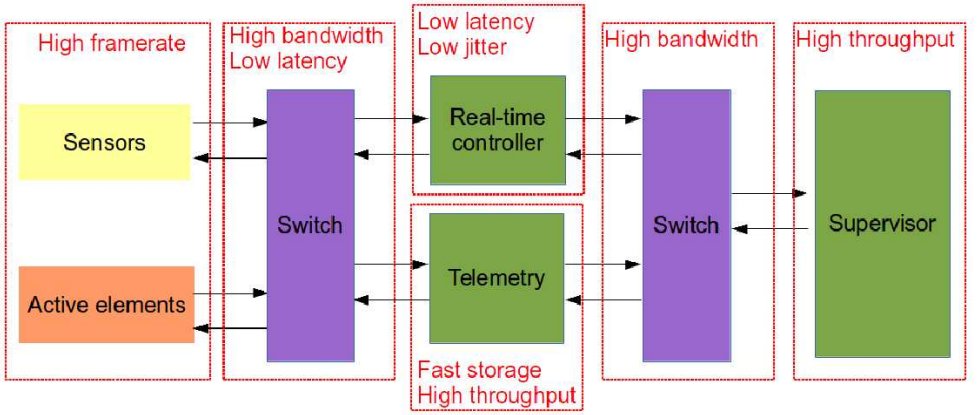
Work Packages interaction



WP2: system management

Task 2.2: System engineering

- General coordination of prototyping activities
- Produce regular progress reports
- Organize mid-term and final reviews



Deliverables

- D2.2a: Prototypes performance mid-term report (OdP – M12)
- D2.2b: Prototypes final performance report (OdP – M24)
- D2.2c: Full scale prototype final design report (OdP – M24)
- D2.2a: Full scale prototype final design report (OdP – M36)

WP2: system management

Coordination meetings since Jan. 2016

Weekly coordination meetings

- between OdP and PLDA (WP 5 & 7)
- between PLDA and UoD (WP 4 & 7)
- between UoD and OdP (WP 4, 6 & 7)

Regular coordination meetings between Mic. and PLDA (WP3)

- Mitigate delay in component procurement
- Including OdP on the long term (WP 3)

Technical cooordination workshops :

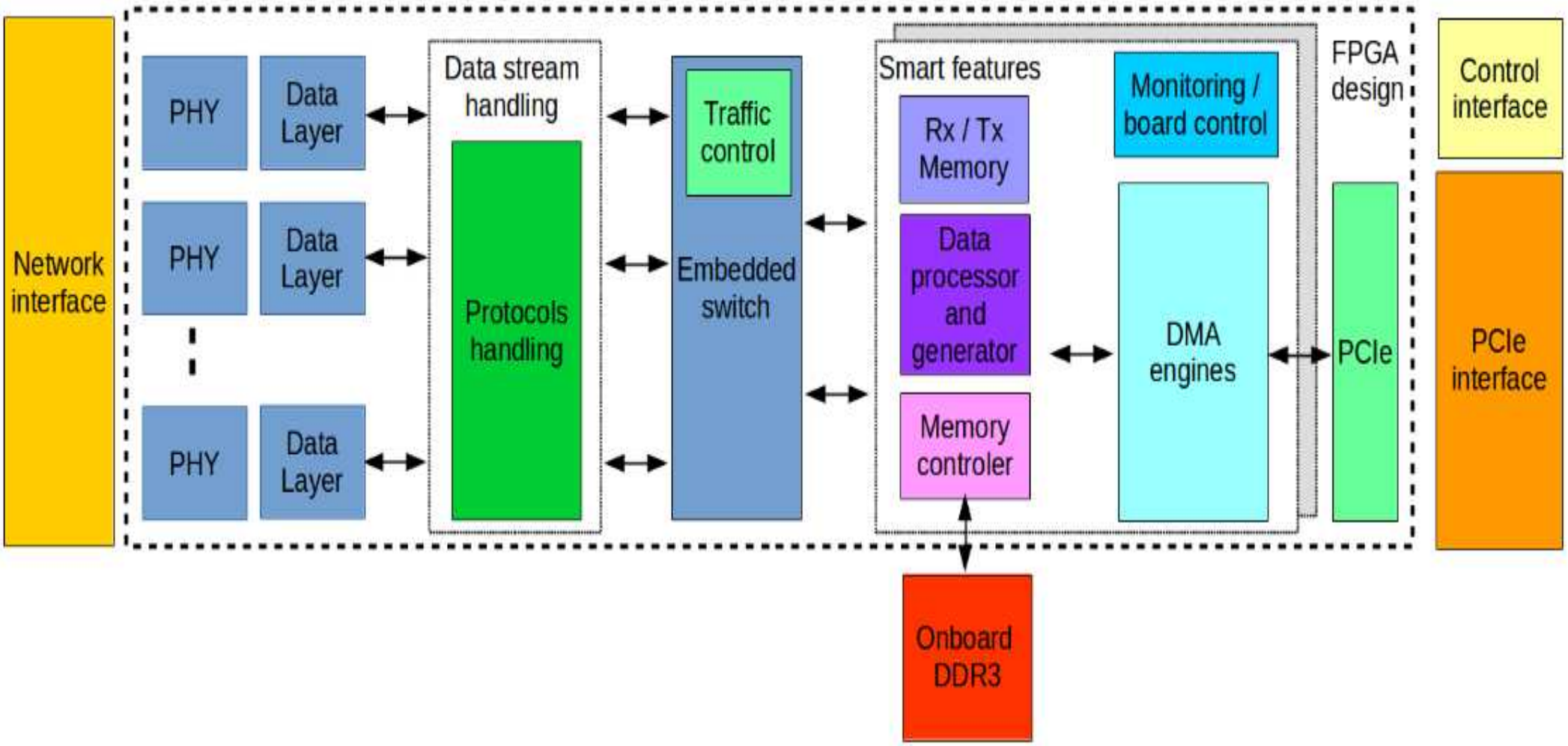
- Mic + PLDA + OdP (Feb. 2016, Jan. 2017)
- Mic + OdP (Nov. 2016)
- PLDA + OdP (May 2016, Jan. 2017)
- OdP + UoD (April 2016, Nov. 2016)

Staff at OdP and start dates

Damien Gratadour – Project lead – 1-Oct-15 (project management)

- Eric Gendron – Project scientist – 1-Oct-15
- Arnaud Sevin – System engineer – 1-Oct-15 (project coordination)
- Denis Perret – FPGA specialist – 1-Oct-15 (FPGA development coordinator)
- Roderick Dembet – SW development – 1-Jan-2016
- Julien Bernard – research engineer SW – 1-Oct-2015 (WP4 lead)
- Florian Ferreira – PhD student – 1-Oct-2015 (WP6 – Simulator validation)
- Maxime Lainé – SW engineer, FPGA development – 1-Oct-2015 (WP4 – WP5 coordination)
- Nicolas Doucet – research engineer SW – 1-Oct-2015 (WP4 – algorithms)
- Sébastien Durand – SW engineer – 1-Jan-2016 (WP6 – simulator)
- Other support: Tristan Buey (project managemment), Julien brulé (sys. admin.)

WP coordination : smart interconnect architecture



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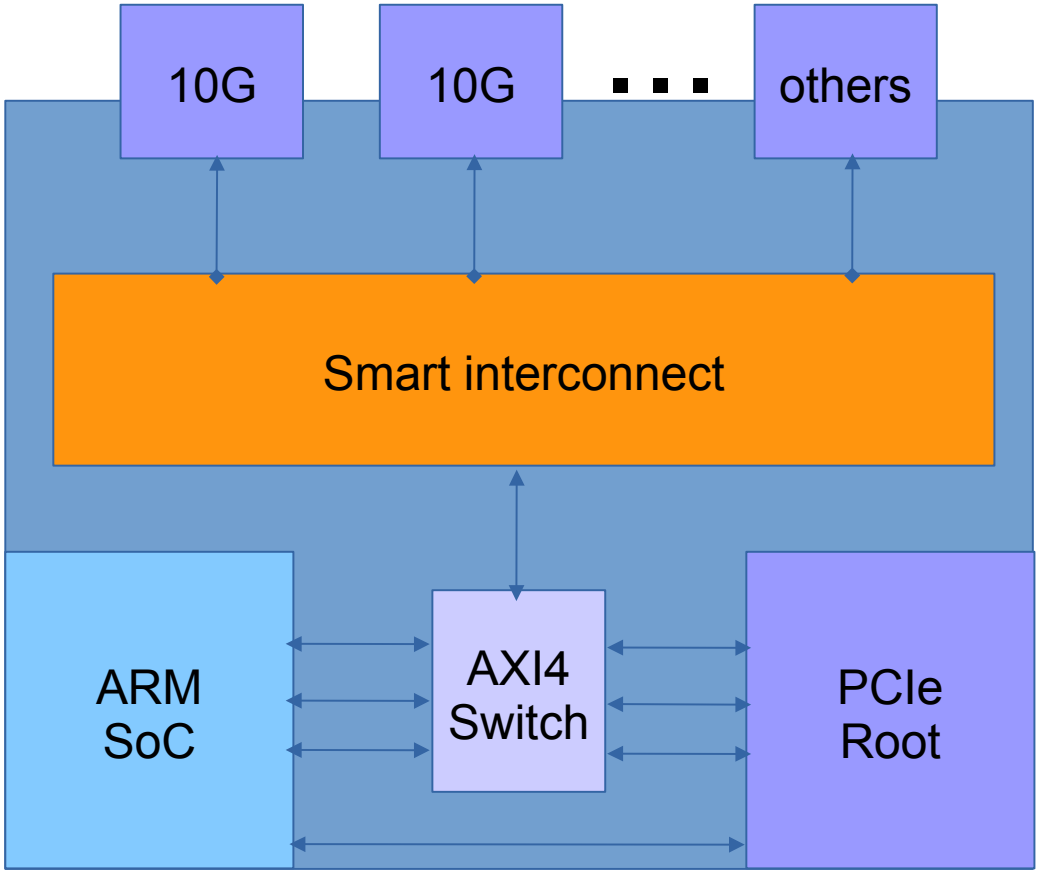
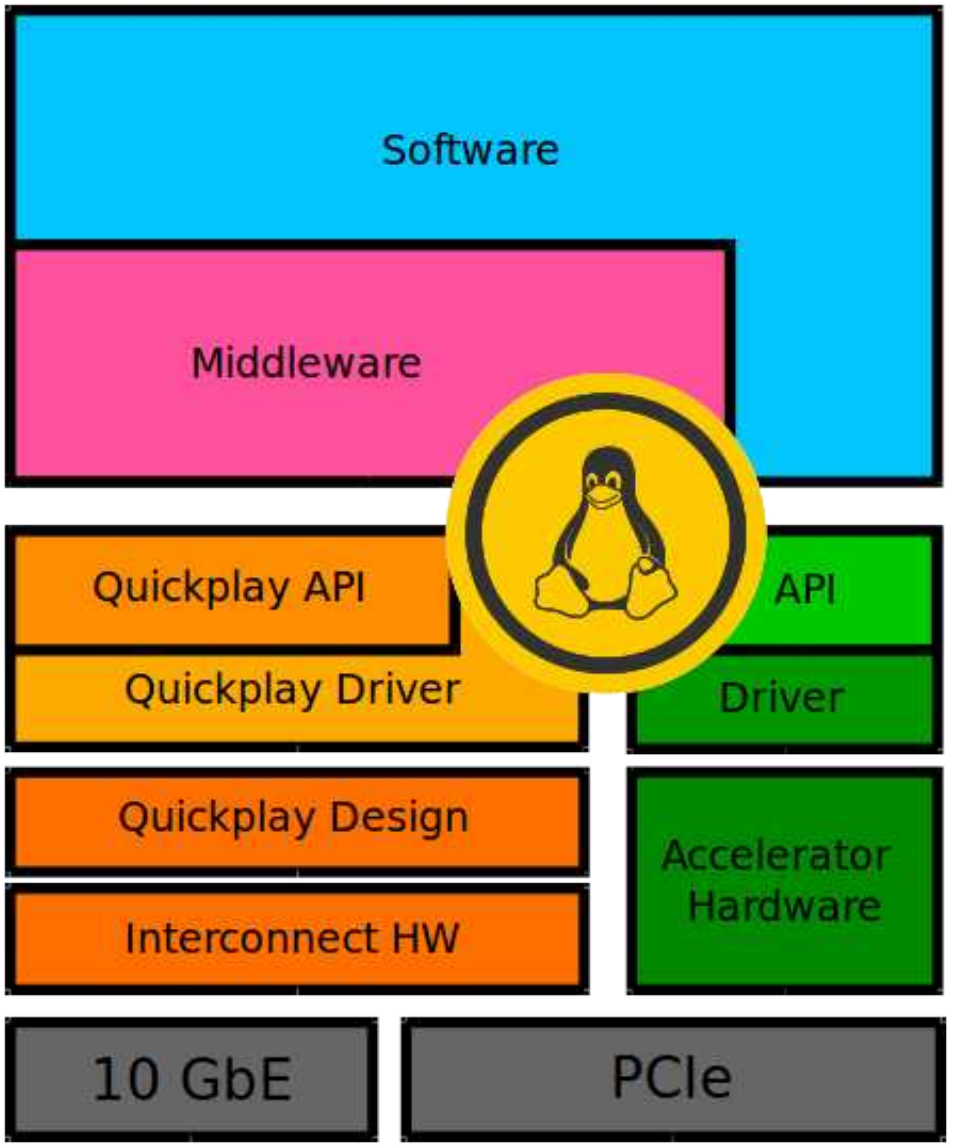
WP coordination : FPGA design of microserver board

- Integration of QuickPlay with Microgate prototype
- Coordination of efforts between 2 European SMEs
- Bring together smart interconnect concept with energy efficient compute platform



SW / MW stack

- Under development
- Run a standard HPC ecosystem on the prototype boards and clusters
- Performance assessed w/r AO application (mainly linear algebra)



Summary

Project on track

- PDR occurred in Jan. 2016 with feedback from community
- Prototyping activities have started with preliminary results (see per WP presentation)

Complex project structure

- Strong effort on OdP side for system management
- Efficient communication channel organized around weekly coordination meetings and JIRA platform + Wiki

Collaborations initiated

- Good feedback from the community on different aspects (HPC + instrumentation)
- Evaluate the convergence and minimize additional effort

More work needed on dissemination

- Populating public website
- Contributions to international conference and publications
- Project presented to SPIE conference on Astronomical Instrumentation (2016)

Already enhancing the readiness level of commercial solutions

- Contribution to QuickPlay development (see Hugues' presentation)
- Design of an innovative FPGA board (see Roberto's presentation)